REMARKS

Claims 1-6 are pending in the present application. New claims 7-16 are added above. Claims 1 and 5 are amended above. No new matter is added by the claim amendments or new claims. Entry is respectfully requested.

The Applicant notes that the Office Action Summary does not indicate whether the drawings filed in the application are acceptable. Confirmation of their acceptability is respectfully requested.

The Applicant further notes that the Office Action Summary does not acknowledge the claim for foreign priority in the application and does not indicate whether a certified copy has been received. Acknowledgment is respectfully requested.

Claims 1-3 stand rejected under 35 U.S.C. 102(b) as being anticipated by Murari, *et al.* (U.S. Patent No. 5,036,269 - hereinafter referred to as "Murari"). Claim 1 stands rejected under 35 U.S.C. 102(b) as being anticipated by Jeon (U.S. Patent No. 5,747,974). Claims 1-6 stand rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art ("AAPA") of this application in view of Bertails, *et al.* (U.S. Patent No. 4,442,398- hereinafter referred to as "Bertails"). Reconsideration and removal of the rejections, and allowance of the claims, are respectfully requested.

In the present invention of amended independent claim 1, an internal voltage generation circuit includes a voltage divider, a comparator, and a driver. The "comparator" is connected to an "external voltage" and an "internal voltage" and the "comparator" compares the divided internal voltage, as divided by the divider, with a reference voltage. The driver is connected to the external voltage and supplies the external voltage to the internal voltage in response to a compared output of the comparator. Hence, when the "external voltage is reduced to a level that is lower than the internal voltage," the "compared output inactivates the driver," whereby the

"driver prevents the supplying of the reduced external voltage to the internal voltage." In this manner, the "internal voltage maintains a constant level."

These features of the present invention of claim 1 are illustrated at least at Figs. 6-8 of the present specification. In this example, a comparator 610 is connected to an external voltage EXT_VDD and an internal voltage IVC (see Fig. 7 and page 7, lines 4-10 of the present specification). A driver 620 is comprised of a PMOS transistor MP11 having a bulk, or back bias voltage, which is connected to a node A of the comparator 610. A source of the PMOS transistor MP11 is connected to the external voltage EXT_VDD (see Figs. 6-7 and page 6, line 21 - page 7, line 1 of the present specification). During normal operation, the external voltage EXT_VDD is higher than the internal voltage IVC, and the voltage at node A of the comparator is the voltage level of the external voltage EXT_VDD (see Fig. 7 and page 8, lines 1-4 of the present specification). In addition, the comparator 610 outputs a "compared output," e.g. a DA_OUT signal, in a logic low state by comparing a divided internal voltage DIV_IVC and a reference voltage VREF (see page 8, lines 4-6 of the present specification). Since the DA_OUT signal is in the logic low state, and is received by the gate of the PMOS transistor MP11, the external voltage EXT_VDD is supplied from the source of the PMOS transistor MP11 to the internal voltage IVC by the PMOS transistor of the driver 620 (see Fig. 7 and page 8, lines 9- 11 of the present specification). However, in the event of a negative external voltage EXT_VDD glitch, the compared output DA_OUT inactivates the driver 620 by turning off the PMOS transistor MP11 of the driver 620, and thereby preventing the external voltage EXT_VDD from being supplied to the internal voltage IVC (see Fig. 7 and page 8, lines 13-16 of the present specification). Here, since the external voltage EXT_VDD is lower than the internal voltage IVC, the voltage level of node A of comparator 610 is the level of the internal voltage IVC and the compared output DA_OUT generated by the comparator is in a logic high state (see FIGs. 6, 7 and 8B and page 8, line 23 to page 9, line 2 of the present specification). Since the compared output DA_OUT of the comparator is in a logic high state in the event of a negative voltage glitch, the PMOS transistor MP11 of the driver 620 is turned off, and the PMOS transistor MP11 therefore prevents the negative voltage glitch generated as the external voltage EXT_VDD from

being transmitted to the internal voltage IVC. In this manner, the internal voltage IVC maintains a constant level despite the negative voltage glitch (see Figs. 7 and 8B and page 9, lines 8-12 of the present specification).

With regard to the rejection of independent claim 1 based on Murari, it is submitted that Murari fails to teach or suggest a "comparator connected to an external voltage and the internal voltage." Murari teaches a voltage stabilizer comprising a first PNP transistor Q1 (referred to in the Office Action at paragraph 2 as a "driver"), a second PNP transistor Q2, and a differential amplifier A (referred to in the Office Action at paragraph 2 as a "comparator"). However, there is no mention in Murari that the differential amplifier A of Murari is connected to both an "external voltage" and an "internal voltage," as claimed. In addition, it is submitted that Murari fails to teach or suggest a "driver connected to the external voltage" wherein "when the external voltage is reduced to a level that is lower than the internal voltage...the driver prevents the supplying of the reduced external voltage to the internal voltage...," as claimed. Instead, Murari teaches a first PNP transistor Q1 having an emitter terminal connected to the collector terminal of a second PNP transistor Q2, and thereby receiving a voltage IN from the second PNP transistor Q2 under normal voltage conditions (see Murari, FIG. 3 and column 4, lines 19-20). However, when a negative voltage peak occurs in Murari, whereby the voltage stabilizer of Murari experiences negative voltage peaks of the "external voltage" (referred to in Murari as an input voltage IN), the second PNP transistor Q2 becomes non-conductive which prevents the input voltage IN from being supplied to node B (see Murari, FIG. 3 and column 5, lines 1-7), and thus the first PNP transistor Q1 does not receive the input voltage IN under these conditions. Here, the capacitor C`` maintains node B at a voltage potential that is sufficient for normal operation of the circuit during the negative voltage peak of the input voltage IN (see Murari, FIG. 3 and column 5, lines 8-11). Therefore, during a negative voltage peak, the first PNP transistor Q1 receives at its emitter a voltage from the capacitor C``, and does not receive an "external voltage" (see Murari, column 5, lines 37-41). There is no mention in Murari that the first PNP transistor Q1 (referred to in the Office Action as a "driver") is "connected to the external voltage," as claimed. Instead, in contrast to the present invention, the first PNP transistor Q1 of

Murari receives a voltage that is discharged from capacitor C`` during a negative voltage peak, and outputs this discharged voltage to the output terminal OUT``. In addition, there is no mention in Murari of a "comparator" that generates a "compared output" to the base of the first PNP transistor Q1, and inactivates the first PNP transistor Q1 during a negative voltage glitch. Therefore, since Murari does not teach or suggest a "comparator connected to an external voltage and the internal voltage," and since the "driver" is not connected to the "external voltage," it follows that Murari fails to teach a "driver connected to the external voltage for supplying the external voltage to the internal voltage in response to the compared output of the comparator," as claimed. In addition, it therefore follows that Murari fails to teach or suggest "when the external voltage is reduced to a level that is lower than the internal voltage...the driver prevents the supplying of the reduced external voltage to the internal voltage," as claimed.

For these reasons, it is submitted that Murari fails to teach or suggest the present invention set forth in amended independent claim 1. Reconsideration and removal of the rejections and allowance of independent claim 1 and dependent claims 2-3 are therefore respectfully requested.

Jeon discloses an internal supply voltage generating circuit that generates internal supply voltages that maintain voltage levels below an external supply voltage (see Jeon, Fig. 5 and Abstract). In Jeon, a first driver 24a is coupled to the output of a first comparator 23a, and a second driver 24b is coupled to the output of a second comparator 23b (see Jeon, Fig. 5).

With regard to the rejection of independent claim 1 based on Jeon, it is submitted that Jeon likewise fails to teach or suggest the invention as claimed in amended independent claim 1. Specifically, it is submitted that Jeon fails to teach or suggest a "comparator" that is connected to both an "external voltage" and an "internal voltage," as claimed. Instead, each comparator 23a, 23b in Jeon is connected to a single voltage, namely external voltage Vext (see Jeon, Fig. 5). Since Jeon does not have an internal voltage supply to the comparator, it follows that Jeon fails to teach or suggest that when a "external voltage is reduced to a level that is lower than the

internal voltage," a "compared output" inactivates the driver. In sum, Jeon discloses a comparator that is similar in structure and operation to that of the conventional embodiment of Fig. 1 of the present specification, as described at page 1, line 10 to page 3, line 20 of the Background section of the present specification. Since Jeon fails to teach or suggest a "compared output" that "inactivates the driver," it follows that Jeon fails to teach or suggest the "driver" that "prevents the supplying of the reduced external voltage to the internal voltage and the internal voltage maintains a constant level," as claimed.

In view of the above discussion, it is submitted that Jeon fails to teach or suggest the present invention as claimed in amended independent claim 1. Therefore, reconsideration and removal of the rejection under 35 U.S.C. 102(b) based on Jeon are respectfully requested.

With regard to the rejection of independent claim 1 in view of the combination of the AAPA and Bertails, it is submitted that the combination fails to teach or suggest the present invention as claimed in amended independent claim 1. AAPA fails to teach or suggest a "comparator connected to an external voltage and the internal voltage," as claimed in amended independent claim 1. Instead, the comparator of AAPA is connected to an external voltage only (see Fig. 3 and page 1, lines 20-21 of the present specification). There is no mention in AAPA of the "comparator" being connected to an "internal voltage." Moreover, AAPA does not teach or suggest that "when the external voltage is reduced to a level that is lower than the internal voltage, the compared output inactivates the driver, and the driver prevents the supplying of the reduced external voltage to the internal voltage and the internal voltage maintains a constant level," as claimed in amended independent claim 1. Instead, in AAPA, when a negative voltage glitch occurs, that is, when the "external voltage is less than the internal voltage," the voltage level of the external voltage EXT_VDD becomes the threshold voltage of the PMOS transistor MP11 of the driver 130, and the PMOS transistor MP11 is turned on (see Figs. 1 and 5B and page 3, lines 11-15 of the present specification). Thus, the glitch of the external voltage EXT_VDD causes a temporary change of the internal voltage IVC since the driver 130 supplies

the glitch of the external voltage EXT_VDD to the internal voltage IVC, and thereby resulting in a semiconductor device malfunction (see page 3, lines 16 - 20 of the present specification).

Bertails is cited in the Office Action at page 3, paragraph 4 is disclosing a first and second diode type NMOS transistor. However, it is submitted that Bertails, like AAPA, fails to teach or suggest a "comparator connected to an external voltage and the internal voltage," as claimed. In addition, Bertails fails to teach or suggest "when the external voltage is reduced to a level that is lower than the internal voltage, the compared output inactivates the driver, and the driver prevents the supplying of the reduced external voltage to the internal voltage and the internal voltage maintains a constant level," as claimed in amended independent claim 1.

Accordingly, it is submitted that AAPA and Bertails, taken alone or in combination, fail to teach or suggest the invention set forth in the amended claims. In particular, neither reference, taken alone or in combination, teaches a "comparator connected to an external voltage and the internal voltage." In addition, neither reference teaches or suggests "when the external voltage is reduced to a level that is lower than the internal voltage, the compared output inactivates the driver, and the driver prevents the supplying of the reduced external voltage to the internal voltage and the internal voltage maintains a constant level," as claimed in amended independent claim 1.

Since the combination of AAPA and Bertails fails to teach or suggest the invention set forth in the amended claims, the claims are believed to be allowable over the cited references. Accordingly, reconsideration and removal of the rejection of claims 1-6 under 35 U.S.C. 103(a) based on AAPA and Bertails are respectfully requested.

With regard to new independent claim 8, it is submitted that none of the references, whether alone or in combination with the others, teaches or suggests "a driver connected to the external voltage for supplying the external voltage to the internal voltage in response to the compared output of the comparator," as claimed in new independent claim 8. In addition, it is

submitted that none of the references teaches or suggests the "driver" comprising "a transistor having a back-bias voltage connected to an internal node of the comparator." as claimed in new independent claim 8. Entry and allowance of claims 8-16 are respectfully requested.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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